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[TITLE OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] TFT ARRAY SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE, AND MANUFACTURING METHODS OF TFT ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE

[CLAIMS]

[CLAIM 1]

A TFT array substrate, comprising:

a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer is formed on the gate electrode via a gate insulation film,

the semiconductor layer having a shape formed by dropping a droplet.

[CLAIM 2]

The TFT array substrate as set forth in claim 1, wherein:

the gate electrode in the thin film transistor section is a branch electrode which is branched out of a main line of the gate electrode, and the branch electrode has an open end protruded from an area for the semiconductor layer.

[CLAIM 3]

The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the source and drain electrodes each have an end that is positioned closer to the channel section, and confined over an entire width within the area for the semiconductor layer.

[CLAIM 4]

The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a light-blocking film on either of an upper layer or an lower layer of the semiconductor layer, the light-blocking film having a shape formed by dropping a droplet, and being formed on a portion corresponding to the position of the semiconductor layer.

[CLAIM 5]

A liquid crystal display device including the TFT array substrate as set forth in claim 1.

[CLAIM 6]

A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode;

(c) depositing a semiconductor film on the gate insulation layer;

(d) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and

(e) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor layer of a thin film transistor section.

[CLAIM 7]

A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode with a branch electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode; and

(c) forming a semiconductor layer having a shape of a

droplet as a semiconductor layer of a thin film transistor section, by dropping a droplet of a semiconductor material on the gate insulation layer on the branch electrode.

[CLAIM 8]

The manufacturing method of a TFT array substrate as set forth in claim 6 or 7, wherein:

in the step (a), the gate electrode is formed so that the gate electrode includes a main line and a branch electrode branched out of the main line, the branch electrode having an open end protruded from an area for the semiconductor layer.

[CLAIM 9]

The manufacturing method of a TFT array substrate as set forth in claim 8, wherein:

the branch electrode is specified by length according to dropping accuracy of the droplet so that the open end is protruded from the area for the semiconductor layer.

[CLAIM 10]

A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode on a substrate;

(b) forming a gate insulation layer on the gate

electrode;

(c) forming a semiconductor layer of a thin film transistor section on the gate insulation layer;

(d) forming a first area to which a source electrode is formed, and a second area to which at least a pixel electrode is formed, by dropping a droplet of an electrode material on the substrate after subjected to the step (c); and

(e) forming a source electrode, a drain electrode, and a pixel electrode in the first and the second areas by dropping droplets of an electrode material on the substrate after subjected to the step (d).

[CLAIM 11]

The manufacturing method of a TFT array substrate as set forth in claim 10, wherein:

the first and the second areas are provided by forming a convex guide which prevents flow of the droplet.

[CLAIM 12]

The manufacturing method of a TFT array substrate as set forth in claim 10, wherein:

the first and the second areas are provided by forming a lyophilic area and a lyophobic area respectively

having a lyophilic characteristic and a lyophobic characteristic with respect to the droplets.

[CLAIM 13]

A manufacturing method of a liquid crystal display device including the manufacturing method of a TFT substrate as set forth in claim 6, 7, or 10.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[INDUSTRIAL FIELD OF THE INVENTION]

The present invention relates to a TFT array substrate, a liquid crystal display device, a manufacturing method of the TFT array substrate, and a manufacturing method of the liquid crystal display device.

[0002]

[PRIOR ART]

Conventionally, for a liquid crystal display device including a TFT (Thin Film Transistor), a TFT array substrate is manufactured through a series of manufacturing steps, as shown in Figure 28. More specifically, the manufacturing method of a conventional TFT array substrate is carried out through the steps of

depositing a material for gate line, forming the gate line, depositing a gate insulation layer and depositing a semiconductor layer, forming the semiconductor layer, depositing a material for source line and drain line, forming the source line and the drain line, processing a channel section, which exists between the source and the drain electrode on the semiconductor layer, forming a passivation film, processing the passivation film, depositing a pixel electrode, and forming the pixel electrode (101 through 111).

[0003]

Among these steps, the gate line forming step 102, the semiconductor layer forming step 104, the source/drain lines forming step 106, the passivation film processing step 109, and the pixel electrode forming step 111, which involves photolithography and etching performed with a mask. More specifically, these steps use photolithography and etching so as to process the film formed through the previous steps, i.e., the gate line depositing step 101, the gate insulation layer/semiconductor layer depositing step 103, the source/drain lines depositing step 105, the passivation

film forming step 108, and the pixel electrode depositing step 110.

[0004]

Meanwhile, there has been a technique proposed in recent years, which forms wiring by an inkjet method without using photolithography. In this technique, the substrate is provided with two areas respectively having an affinity characteristic and a non-affinity characteristic with respect to a liquid material of the wiring, in a surface to which the wiring will be formed; and the liquid of the wiring material is dropped by an inkjet method onto the affinity area so as to form the wiring. Hereinafter, the areas having an affinity characteristic and a non-affinity characteristic with respect to a general liquid including a liquid wiring material are referred to as a lyophilic area and a lyophobic area, respectively; and the areas having an affinity characteristic and a non-affinity characteristic with respect to an aqueous liquid are referred to as a hydrophilic area and a hydrophobic area, respectively. Such a technique is disclosed in Japanese Laid-Open Patent Application Tokukaihei 11-204529/1999.

[0005]

Further, another wiring forming technique using an inkjet method is disclosed in Japanese Laid-Open Patent Application Tokukai 2000-353594/2000. In this method, the wiring forming area is provided with banks on the respective ends so as to keep the wiring material within the area. In this technique, the upper portion of the bank is lyophobic, and the wiring forming area is lyophilic.

[0006]

Further, still another wiring forming technique using an inkjet method is disclosed in SID 01 DIGEST, Page 40 to 43, 6.1: Invited Paper: A11-Polymer Thin Film Transistors Fabricated by High-Resolution Inkjet Printing (by Takeo Kawase and other writers) in which a TFT is formed only by organic materials.

[0007]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

As described, the conventional manufacturing method of a TFT array substrate involving photolithography uses masks at least in the following five steps: the gate line forming step 102, the semiconductor layer forming step 104, the source/drain lines forming

step 106, the passivation film processing step 109, and the pixel electrode forming step 111. Further, the conventional method uses vacuum equipments in the respective deposition steps, and also in the respective processing steps (forming and processing steps) after the deposition. Accordingly, in order to meet the recent market demand for a larger liquid crystal display device, the conventional method consumes enormous cost, as the TFTs are formed by such a manner with respect to a large-sized substrate.

[0008]

Furthermore, the demand for a larger substrate brings about greater consumption of resists or wiring material. Meanwhile, the materials (such as a resist) used in the processing steps for forming the wiring etc., are removed and discarded by etching or removing, since an effective reusing method of those has not yet been realized. Accordingly, works and costs for the discard are growing bigger with the demand for a larger substrate, as well as environmental burden due to the discarded material. As described, the conventional manufacturing method of a TFT array substrate, which mainly involves

photolithography, requires more manufacturing steps and a greater cost.

[0009]

On the other hand, as disclosed in the foregoing Documents, the manufacturing method of a TFT array substrate using an inkjet method requires less number of masks. Therefore, there has been a demand for development of the inkjet method as a technique for realizing reduction in both manufacturing steps and costs.

[0010]

[MEANS TO SOLVE THE PROBLEMS]

In order to solve the above problem, a TFT array substrate according to the present invention includes: a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer is formed on the gate electrode via a gate insulation film, the semiconductor layer having a shape formed by dropping a droplet.

[0011]

With this arrangement, since the semiconductor layer has a shape of a dropped droplet(s) (substantially a circular shape, or a shape made of plural overlapped

circles, for example), the semiconductor layer can be formed by dropping a droplet(s) of a semiconductor material by using an inkjet method. Alternatively, the semiconductor layer may be formed in such a manner that a resist layer is formed by dropping a droplet(s) of a resist material onto a semiconductor film by an inkjet method, and the resist layer is used as a mask for processing a semiconductor film.

[0012]

With this method, it is possible to manufacture the TFT array substrate without a mask for forming a semiconductor layer. Accordingly, the required number of masks in the manufacturing is reduced, thus reducing manufacturing processes. Further, the manufacturing requires less photolithography processes using a mask, thus reducing equipment outlay for the photolithography. On this account, it is possible to reduce the time and costs of manufacturing.

[0013]

Note that, in addition to the foregoing inkjet method, the dropping of the droplet of a semiconductor material or a resist material can be carried out by any methods

enabling direct formation of the semiconductor layer or the resist layer, by dropping a droplet(s).

[0014]

The TFT array substrate may have such an arrangement that the gate electrode in the thin film transistor section is a branch electrode which is branched out of a main line of the gate electrode, and the branch electrode has an open end protruded from an area for the semiconductor layer.

[0015]

With the foregoing arrangement, since the open-end of the branch electrode of the thin film transistor section is protruded from the area for the semiconductor layer, a leak current between the source and drain electrodes can be appropriately suppressed by the electrical field from the branch electrode.

[0016]

The foregoing TFT array substrate may have such an arrangement that the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the source

and drain electrodes each have an end that is positioned closer to the channel section, and confined over an entire width within the area for the semiconductor layer.

[0017]

With the foregoing arrangement, the source electrode of each pixel can be supplied with a sufficient ON current, thus preventing nonuniformity of charging condition of the pixel, which causes unevenness of the image.

[0018]

The TFT array substrate according to the present invention may have such an arrangement that the thin film transistor section further includes a light-blocking film on either of an upper layer or an lower layer of the semiconductor layer, the light-blocking film having a shape formed by dropping a droplet, and being formed on a portion corresponding to the position of the semiconductor layer.

[0019]

With the foregoing arrangement, when the light-blocking film is required, it can be created easily by dropping a droplet(s) of a light-blocking film material by using an inkjet method or the like. Accordingly, as with

the forming of the semiconductor layer, the light-blocking film can be formed without a mask. On this account, it is not necessary to use extra number of masks or larger amount of material in the manufacturing of the TFT array substrate, thus reducing manufacturing steps and costs.

[0020]

The liquid crystal display device of the present invention includes the foregoing TFT array substrate. Therefore, the manufacturing of the liquid crystal display requires less number of masks, thus reducing time and costs of manufacturing.

[0021]

A manufacturing method of a TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; (c) depositing a semiconductor film on the gate insulation layer; (d) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and (e) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor

layer of a thin film transistor section.

[0022]

In this manner, a resist layer is formed on a deposited semiconductor film by dropping a droplet of a resist material, and the semiconductor layer is formed by using this resist layer having the shape of the droplet (normally a circular shape) as a mask.

[0023]

With this method, it is possible to manufacture the TFT array substrate without a mask for forming a semiconductor layer. Accordingly, the required number of masks in the manufacturing is reduced, thus reducing manufacturing processes. Further, the manufacturing requires less photolithography processes using a mask, thus reducing equipment outlay for the photolithography. On this account, it is possible to reduce the time and costs of manufacturing.

[0024]

Note that, in addition to the foregoing inkjet method, the dropping of the droplet of a resist material can be carried out by any methods enabling direct formation of the resist layer by dropping a droplet(s).

[0025]

A manufacturing method of a TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; and (c) forming a semiconductor layer having a shape of a droplet as a semiconductor layer of a thin film transistor section, by dropping a droplet of a semiconductor material on the gate insulation layer.

[0026]

In this manner, the semiconductor layer is formed in a shape of a droplet (normally a circular shape) by only dropping a droplet of a semiconductor material on the gate insulation layer of the branch electrode.

[0027]

With this method, it is possible to manufacture the TFT array substrate without a mask for forming a semiconductor layer. Accordingly, the required number of masks in the manufacturing is reduced, thus reducing manufacturing processes. Further, the manufacturing requires less photolithography processes using a mask, thus reducing equipment outlay for the photolithography

and amount of waste material. On this account, it is possible to reduce the time and costs of manufacturing, and to effectively use the materials.

[0028]

Note that, in addition to the foregoing inkjet method, the dropping of the droplet of a semiconductor material can be carried out by any methods enabling direct formation of the semiconductor layer by dropping a droplet(s).

[0029]

The manufacturing method of a TFT array substrate may have such an arrangement that in the step of forming the gate electrode, the gate electrode is formed having a main line and a branch electrode which is branched out of the main line, and the branch electrode has an open end protruded from an area for the semiconductor layer.

[0030]

With the foregoing arrangement, since the open-end of the branch electrode of the thin film transistor section is protruded from the area for the semiconductor layer, a leak current between the source and drain electrodes can be appropriately suppressed by the electrical field from

the branch electrode.

[0031]

The foregoing manufacturing method of the TFT array substrate may be arranged so that: the branch electrode is specified by length according to dropping accuracy of the droplet so that the open end is protruded from the area for the semiconductor layer.

[0032]

In this manner, the droplet of a resist material or a semiconductor material is dropped in a position for allowing the open-end of the branch electrode to be protruded from the area for the completed semiconductor. Thus, the leak current between the source and drain electrodes can be appropriately suppressed.

[0033]

A manufacturing method of a TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; (c) forming a semiconductor layer of a thin film transistor section on the gate insulation layer; (d) forming a first area to which a source electrode is formed, and a second area to which

at least a pixel electrode is formed, by dropping a droplet of an electrode material on the substrate after subjected to the step (c); and (e) forming a source electrode, a drain electrode, and a pixel electrode in the first and the second areas by dropping droplets of an electrode material on the substrate after subjected to the step (d).

[0034]

In this manner, the first area to which a source electrode is formed by dropping a droplet of an electrode material, and the second area to which at least a pixel electrode is formed by dropping a droplet of an electrode material are formed in one process for pre-processing of the electrode forming step. Therefore, the manufacturing processes and costs can be reduced compared to the case of separately forming the first and the second areas in different steps.

[0035]

In the above manufacturing method of a TFT array substrate, the first and the second areas may be provided by forming a convex guide which prevents flow of the droplet. Alternatively, the first and the second areas may be provided by forming a lyophilic area and a lyophobic

area having a lyophilic characteristic and a lyophobic characteristic with respect to the droplets.

[0036]

A manufacturing method of a liquid crystal display device according to the present invention includes one of the foregoing manufacturing methods of a TFT array substrate. Therefore, it is possible to reduce at least manufacturing processes for producing a liquid crystal display device.

[0037]

[EMBODIMENTS]

[FIRST EMBODIMENT]

One Embodiment of the present invention is described below with reference to Figures 1 through 13.

A liquid crystal display device according to the present Embodiment includes a pixel shown in Figure 1(a). Note that, Figure 1(a) is a plan view showing a schematic configuration of a pixel of a TFT array substrate in the liquid crystal display device. Further, Figure 1(b) is a cross-sectional view, taken along the line A-A of Figure 1(a).

[0038]

As shown in Figures 1(a) and 1(b), a TFT array substrate 11 is made of a glass substrate 12 on which a gate electrode 13 and a source electrode 17 are aligned in a matrix manner. A storage capacitor electrode 14 is provided between two adjacent gate electrodes 13.

[0039]

As shown in Figure 1(b), in the TFT array substrate 11, the gate electrode 13 and the storage capacitor electrode 14 are provided on the glass substrate 12 in an area between a TFT section 22 and an storage capacitor section 23; and a gate insulation layer 15 is further provided thereon.

[0040]

Further, a semiconductor layer 16 including an a-Si layer is formed on the gate electrode 13 via the gate insulation layer 15, and the source electrode 17 and a drain electrode 18 are further formed thereon. One end of the drain electrode 18 extends to an area on the storage capacitor electrode 14 by having the gate insulation layer 15 underneath, and a contact hole 24 is formed on this area. A passivation film 19 is formed on the source electrode 17 and the drain electrode 18, and a

photosensitive acrylic resin layer 20 and a pixel electrode 21 are further formed thereon in this order.

[0041]

In the present Embodiment, manufacturing of the TFT array substrate 11 is performed with a pattern forming equipment. This pattern forming equipment discharges or drops material of the layer with an inkjet method, for example. As shown in Figure 2, the pattern forming equipment includes a supporting stage 32 on which a substrate 31 (corresponding to the glass substrate 12) is placed. The pattern forming equipment includes an inkjet head 33 as droplet discharging means for discharging, for example, fluid ink (droplet) containing a wiring material, with respect to the surface of the substrate 31 placed on the supporting stage 32, and an X-direction driving section 34 for moving the inkjet head 33 in the X-direction, as denoted in the figure, and a Y-direction driving section 35 for moving the inkjet head 33 in the Y-direction of the figure.

[0042]

Further, the pattern forming equipment includes an ink supplying system 36 for supplying ink to the inkjet

head 33, and also includes a control unit 37. The control unit 37 performs various controls including driving control for the X-direction driving section 34 and the Y-direction driving section 35, and discharge control for the inkjet head 33. The control unit 37 supplies information for indicating the position where the ink is applied, with respect to the X and Y-direction driving sections 34 and 35, and supplies discharge information to a head driver (not shown) of the inkjet head 33. With this arrangement, the inkjet head 33 is shifted by the X-direction driving section 34 and Y-direction driving section 35 so that the substrate 31 is provided with desired amount of droplet in a target position on its surface.

[0043]

The inkjet head 33 may be of a piezo-type using a piezoactuator, a bubble-type including a heater in the head, or the like. The discharge amount of the inkjet head 33 may be controlled according to an application voltage. Further, the droplet discharging means may be any means capable of supplying a droplet; therefore, the inkjet head 33 may instead be a device having only a

droplet dropping function, for example.

[0044]

Next, the following will explain a manufacturing method of the TFT array substrate 11 for a liquid crystal display device according to the present Embodiment.

[0045]

In the present Embodiment, the TFT array substrate 11 is manufactured through, as shown in Figure 3, a gate pre-processing step 41, a gate line applying/forming step 42, a gate insulation layer/semiconductor layer depositing step 43, a semiconductor layer forming step 44, a source/drain lines pre-processing step 45, a source/drain lines applying/forming step 46, a channel section processing step 47, a passivation film forming step 48, a passivation film processing step 49, and a pixel electrode forming step 50.

[0046]

(Gate pre-processing step 41)

The gate pre-processing step 41 is performed as a pre-processing of the gate line applying/forming step 42. The gate line applying/forming step 42 as the following step is performed for forming a gate line by dropping

liquid wiring material with a pattern forming equipment. Therefore, this step carries out preparation for appropriate liquid wiring material application, i.e., appropriate discharging (dropping) of the liquid wiring material from a pattern forming equipment with respect to a gate line forming area 61 shown in Figure 4(a). Note that, Figure 4(a) is a plan view of a glass substrate 12 included in the TFT array substrate 11.

[0047]

This step falls roughly into two processes. In hydrophilic/hydrophobic processing (lyophilic/lyophobic processing) as the first process, the substrate is provided with either lyophilic characteristic or lyophobic characteristic with respect to the liquid wiring material, so as to pattern a hydrophilic (lyophilic) area as an area for forming the gate line 61, and a hydrophobic (lyophobic) area as an area for not forming a gate line. In a guide forming process as the second step, the substrate is provided with guides along the gate line forming area 61, for controlling flow of the liquid.

[0048]

The first step, i.e., the hydrophilic/hydrophobic

processing is typically performed by a photocatalyst containing titanium oxide. The second step, i.e., the guide forming is performed by photolithography using a resist material. Occasionally, the guide or the surface of the substrate may be exposed to CF_4/O_2 plasma so as to obtain hydrophilic/hydrophobic characteristics. The resist is removed after the wiring is formed.

[0049]

In the present Embodiment, the hydrophilic/hydrophobic processing was performed by a photocatalyst using titanium oxide, as described below. The glass substrate 12 of the TFT array substrate 11 was coated with a ZONYL FSN (Product Name: provided by Dupont-TORAY Co.ltd), which is a fluorochemical nonionic surfactant which had been mixed with an isopropyl alcohol. Further, a mask of the pattern for the gate electrode was provided with a photocatalyst layer by subjecting the mask spin-coating with a mixture containing titanium dioxide particle dispersing element and an ethanol, and then by baking the mask at 150°. Next, the glass substrate 12 was exposed to ultraviolet light with the mask. This exposure was performed for

two minutes using irradiation of ultraviolet light of 365nm on condition of 70mW/cm^2.

Here, when it is predicted that the semiconductor layer 16 on the glass substrate 12 is exposed to intensive light, a light blocking film 62 may be formed in advance, as shown in Figure 4(a), so as to prevent the semiconductor layer 16 from the light. The light blocking film 62 is formed by dropping the material of film by a pattern forming equipment with respect to a position where an a-Si layer is formed, and then by baking the dropped material. This material of the film may be a photosensitive resin or a thermosetting resin, which is mixed with a black colored material such as a carbon black or TiN.

[0050]

(Gate line applying/forming step 42)

Figures 4(b) and 4(c) show the gate line applying/forming step 42. Figure 4(b) is a plan view of the glass substrate 12 provided with the gate electrode 13, and Figure 4(c) is a cross-sectional view, taken along the line B-B of Figure 4(b).

[0051]

In this step, as shown in Figures 4(b) and 4(c), a material of wiring is applied onto the gate line forming area 61 on the glass substrate 12 with a pattern forming equipment. In this Embodiment, an organic solvent in which Ag particles coated with an organic film are dispersed was used as the wiring material. The wiring width was adjusted to approximately 50μm, and discharge amount of the wiring material from the inkjet head 33 was adjusted to 80pl.

[0052]

In the area processed to have hydrophilic/hydrophobic characteristics, the wiring material discharged from the inkjet head 33 spreads along the gate line forming area 61, and therefore, the space between each discharging of the wiring material was adjusted to approximately 500μm. After the discharging, the material was baked for an hour with a baking temperature of 350°C so as to complete the wiring of the gate electrode 13.

[0053]

Note that, the baking temperature of 350°C in this example was determined in consideration of the coming

semiconductor layer forming step 44 in which processing heat of about 300°C will be added. Thus, the baking temperature is not limited to this temperature. For example, in case of forming an organic semiconductor, the baking temperature may be decreased to a range from 200 to 250°C, if the annealing temperature is set to 100 to 200°C.

[0054]

Further, in addition to Ag, the wiring material may also be Ag-Pd, Ag-Au, Ag-Cu, Cu, Cu-Ni etc. These materials may be individually adopted, or in a form of particles of an alloy material, or as a paste dissolved in an organic solvent. Further, each dissociation temperature of the coating layer on the surface of the particles and the organic material dissolved in the solvent may be controlled according to the required baking temperature so that the wiring material has a desired resistance value and surface condition. Note that, the dissociation temperature designates a temperature for causing vaporization of the coating layer on the surface and the solvent.

[0055]

(Gate insulation layer/semiconductor layer depositing step 43)

Figure 5(a) shows the gate insulation layer/semiconductor layer depositing step 43. In this step, the gate insulation layer 15, the a-Si forming layer 64, and the n+ forming layer 65 are continuously formed in this order on the glass substrate 12, which has been through the gate line applying/forming step 42. In this Embodiment, the a-Si forming layer 64 was made by a CVD method. The thicknesses of the gate insulation layer 15, the a-Si forming layer 64, and the n+ layer 65 are set to 0.3μm, 0.15μm, and 0.04μm, respectively, and each layer was formed continuously without taking the substrate from the vacuum equipment. The deposition temperature was 300°C.

[0056]

(Semiconductor layer forming step 44)

Figures 5(b) through 5(e) show the semiconductor layer forming step 44. Figure 5(e) is a plan view showing the glass substrate 12 after the semiconductor layer forming step 44, Figure 5 (d) is a cross-sectional view, taken along the line C-C of Figure 5(e), and Figures 5(b)

and 5(c) are cross-sectional views showing respective processes in the portion of Figure 5(d).

[0057]

In this step, as shown in Figure 5(b), a thermosetting resin as the resist material was dropped from a pattern forming equipment onto the n+ layer 65 in a portion right above a TFT section gate electrode (branch electrode) 66, which is branched out from the main line of the gate electrode 13. The resin thus applied by dropping was then formed to be a resist layer 67, which is used as a processing pattern. The discharging amount of the resist material was a 10pl droplet. As a result, a circular pattern with a diameter = 30μm was formed on a predetermined position above the TFT section gate electrode 66. Then the pattern was baked with the baking temperature of 150°C. As to the thermosetting resin for forming the resist layer 67, the present Embodiment used a resist of TEF series (provided by Tokyo Ohka Kogyo co. ltd.) whose viscosity had been adjusted in advance to be used for an inkjet method.

[0058]

Note that, in addition to the thermosetting resin, an

UV resin or a photoresist may also be used as the material of the resist layer 67. Further, though it is not a required condition, a transparent resist layer 67 makes positioning upon forming easier. Further, it is preferable that the resist layer 67 is resistant to the heat upon etching, resistant to dry etching gas, and has good selectivity to etching materials.

[0059]

Next, as shown in Figure 5(c), the n+ forming layer 65 and the a-Si forming layer 64 were subjected to dry etching using a gas (such as SF6↓+HC1) so as to form an n+ layer 69 and an a-Si layer 68. Thereafter, the glass substrate 12 was washed by an organic solvent, and the resist layer 67 was removed, as shown in Figure 5(d).

[0060]

As described, in the semiconductor layer forming step 44, the resin pattern (the pattern of the resist layer 67) discharged from a pattern forming equipment determines the shape of the semiconductor layer 16 which is made up of the n+ layer 69 and the a-Si layer 68. Namely, the semiconductor layer 16 is formed as a circular or substantially a circular pattern made up of a

curved line, according to the shape of the material of the resist layer 67 dropped on the glass substrate 12 from the inkjet head 33.

[0061]

Though the resist layer 67 of this embodiment is formed by s single droplet with a pattern forming equipment, the resist layer 67 may also be formed by plural droplets. However, it should be noted that, when the resist layer 67 is formed by a plurality of extremely small droplets, forming of a semiconductor layer 16 takes a long period of time, and also the life of the inkjet head 33 is shortened as more dot number is required.

[0062]

When forming a desirable size of layer (film) by dropping droplets with the inkjet head 33, it is important to drop an appropriate amount of droplet with a minimum number of shots. In this way, it is possible to carry out maximum number of processings within the life period of the inkjet head 33, thus minimizing device cost.

[0063]

Further, as another noticeable characteristic of the semiconductor layer forming step 44, no particular

processing is necessary for the surface to be supplied with droplets discharged from the inkjet head 33. More specifically, if the surface to be supplied with droplets is significantly hydrophilic, the discharged droplet will spread in an infinite form unless the surface is patterned. In such a condition, the film forming cannot be performed. However, since it contains a large number of Si dangling bonds, the a-Si forming layer 64 is basically hydrophobic. Therefore, the droplet is applied on the a-Si forming layer 64 with a certain large degree of contact angle, and results in a substantially circular shape. Accordingly, no particular processing is required for the substrate (a-Si forming layer 64).

[0064]

Further, a substrate which has been subjected to baking or processing in a gas (dry etching) etc. often has substances in a form of a short molecular on its surface. Therefore, the discharged droplet is likely to forms a certain large degree of contact angle, even when using other semiconductor than a-Si, such as an organic semiconductor.

[0065]

Conventionally, patterning of a semiconductor layer requires a mask and photolithography processing. However, in the semiconductor layer forming step 44, the mask pattern is directly drawn with a droplet dropped from the inkjet head 33, thus not requiring a mask and photolithography processing. Therefore, by adopting this step, manufacturing cost can be greatly reduced.

[0066]

(Source/drain lines pre-processing step 45)

Figure 6(a) shows the source/drain lines pre-processing step 45. Figure 6(a) is a plan view showing the glass substrate 12 which has been through the semiconductor layer forming step 44, and provided with a wiring guide 71 for forming the source and drain electrodes 17 and 18.

[0067]

In this step, the wiring guide 71 is formed on an area (source/drain forming area 73) on which the source electrode 17 and the drain electrode 18 and the drain electrode 18 will be formed. In this Embodiment, the wiring guide 71 was formed by a photoresist material. More specifically, the glass substrate 12 after the

semiconductor layer forming step 44 was coated with a photoresist, subjected to pre-baking, exposed using a photo mask, developed, and then subjected to post-baking. The wiring guide 71 thus created had a width = 10μm, and the width of the groove (the width of the wiring forming area) created with the wiring guide 71 was approximately 15μm. Note that, the interval between the source and drain electrodes, i.e., the channel section 72 was set to 4μm.

[0068]

Note that, here, the glass substrate 12 may be arranged such that the SiNx surface (the upper surface of the gate insulation layer 15) is processed to have hydrophilicity by an oxygen plasma, and the wiring guide 71 is processed to have water-repellence by exposing to CF_4 plasma, so that the wiring material from a pattern forming equipment can be smoothly applied to the base surface.

[0069]

Further, instead of forming the wiring guide 71, the glass substrate 12 may be subjected to the hydrophilic/hydrophobic processing using a photocatalyst

according to the pattern of wiring electrode, as with the foregoing gate electrode forming step.

[0070]

(Source/drain lines applying/forming step 46)

Figures 6(b) and 6(c) show the source/drain lines applying/forming step 46. Figure 6(b) is a plan view showing the source and drain electrodes 17 and 18 which are formed along the wiring guide 71, and Figure 6(c) is a cross-sectional view, taken along the line D-D of Figure 6(b).

[0071]

As shown in Figures 6(b) and 6(c), in this source/drain lines applying/forming step 46, the source electrode 17 and the drain electrode 18 were formed by coating the source/drain forming area 73, which is formed by the wiring guide 71, with a wiring material by using a pattern forming equipment. Here, the discharging amount of the wiring material from the inkjet head 33 was set to 2pl. Further, Ag particles are used as the wiring material, and the thicknesses of the electrodes were adjusted to 0.3μm. Further, baking temperature was 200°C, and after the baking, the wiring guide 71 was

removed by an organic solvent.

[0072]

Note that, in this step, the same wiring material may be used as the one used for the gate electrode 13; however, the baking temperature is required to be at or lower than 300°C, since the a-Si is formed at around 300°C.

[0073]

Then, the basic structure of a TFT is almost completed by thus being through the Gate pre-processing step 41 through the source/drain lines applying/forming step 46.

[0074]

Here, in the TFT section 22, it is important that the TFT gate electrode 66 of the gate electrode 13 penetrates through the semiconductor pattern (a semiconductor layer 16) having substantially a circular shape, as shown in Figure 7. In an arrangement in which the TFT section gate electrode 66 is formed within the semiconductor pattern, a leak current will flow between the source and drain electrodes through a semiconductor area on which the electrical field from the TFT section gate electrode 66 does not sufficiently affect, even if the gate is OFF. This

phenomenon will be described later in detail. Note that, in the practical use of the TFT, the foregoing structure generates desirable photoconductor even though the semiconductor pattern is extending out of the TFT section gate electrode 66, the source electrode 17, and the drain electrode 18.

[0075]

(Channel section processing step 47)

This step is carried out for processing the channel section 72, as shown in Figures 8(a) and 8(b). Figures 8(a) and 8(b) are cross-sectional views corresponding to a portion taken along the line D-D of Figure 6(b). Firstly, as shown in Figure 8(a), the wiring guide 71 of the channel section 72 was removed by an organic solvent or by ashing. Next, as shown in Figure 8(b), the n+ layer 69 was subjected to oxidation treatment by ashing or by using a laser so as to be a nonconductor.

[0076]

(Passivation film forming step 48, Passivation film processing step 49)

In this step, as shown in Figures 9(a) and 9(b), a SiO_2 film as a passivation film 19 was formed by a CVD on

a glass substrate 12 which had been provided with the source and drain electrodes.

[0077]

Next, the SiO_2 film was coated with an acrylic resist material so as to create a photosensitive acrylic resin layer 20, and then a pixel electrode forming pattern (see Figure 9(b)) and a terminal processing pattern were formed in this resist layer.

[0078]

The pixel electrode pattern and the terminal processing pattern were formed by a mask for creating a portion where the resist layer is completely removed, and a portion where the resist layer is removed by a half of the thickness, after the development. The latter portion is an area for halftone exposure, whose transmittance of mask is 50%. More specifically, the resist layer is completely removed in the portion for forming a terminal by subjecting the passivation film 19 and the gate insulation layer 15 to etching, and meanwhile, the resist layer is removed to be half in thickness in the portion for forming a pixel electrode 21 so as to create a guide with the photosensitive acrylic resin layer 20 in the periphery of

the pixel electrode pattern. Next, by using the resist layer as a mask, the passivation film 19 and the gate insulation layer 15 in the terminal section were removed, and the passivation film 19 in the portion for forming a pixel electrode 21 were partly removed by etching.

[0079]

(Pixel electrode forming step 50)

As shown in Figures 10(a) and 10(b), the pixel electrode forming pattern on the photosensitive acrylic resin layer 20 was coated with an ITO particle material for creating a pixel electrode by using a pattern forming equipment, and then was baked with a temperature of 200°C so as to form a pixel electrode 21. Here, a TFT array substrate 11 is completed.

[0080]

Conventional photolithography requires a mask in both the passivation film processing and an ITO processing, respectively. On the other hand, by carrying out halftone exposure with a photosensitive acrylic resin, those processings can be carried out with a single mask, thus reducing the manufacturing cost.

[0081]

Here, with reference to Figures 11(a) and 11(b), and Figures 12(a) and 12(b), the following will explain the generation mechanism of a leak current, which was mentioned in the source/drain lines applying/forming step 46.

[0082]

Figure 11(a) is a plan view showing the TFT section with the TFT section gate electrode 66 penetrating through the semiconductor pattern (semiconductor layer 16), and Figure 11(b) is a cross-sectional view, taken along the line G-G of Figure 11(a). Figure 12(a) is a plan view showing the TFT section with the TFT section gate electrode 66 not penetrating through the semiconductor pattern and is provided within the semiconductor pattern area. Figure 12(b) is a cross-sectional view, taken along the line H-H of Figure 12(a). Further, Figures 11(a) and 12(a) show a state where a negative potential is applied to the gate electrode 13. As shown in Figures 11(b) and 12(b), the TFT section gate electrode 66 and the a-Si layer 68 are opposed to each other having the gate insulation layer 15 therebetween. Here, the n+ layer 69 is a layer to inject carriers into the a-Si layer 68, and provided with an

excessive number of electrons through doping of such as a phosphorous (P).

[0083]

For the respective TFTs shown in Figures 11(a) and 11(b) (the TFT section gate electrode 66 penetrating through the semiconductor pattern), and Figures 12(a) and 12(b) (the TFT section gate electrode 66 not penetrating through the semiconductor pattern), a voltage of -4V was applied to the gate electrode, and a leak current between the source and drain electrodes were measured. The measurement came out as: the leak current in the TFT section gate electrode 66 penetrating through the semiconductor pattern was approximately 1pA. Meanwhile, the leak current in the TFT section gate electrode 66 not penetrating through the semiconductor pattern increased to 30 to 50pA.

[0084]

The measurement was carried out under dark circumstances, and in the presence of irradiation of a backlight, the leak current in the TFT section gate electrode 66 penetrating through the semiconductor pattern increased to 20pA. Meanwhile, the leak current

in the TFT section gate electrode 66 not penetrating through the semiconductor pattern greatly increased to approximately 2000 to 3000pA. These results show that the TFT characteristic deteriorates in the arrangement with the TFT section gate electrode not penetrating through the semiconductor pattern. Further, reasons for those results may be explained as follows.

[0085]

Firstly, the following will explain the case where a negative potential is applied to the gate electrode 13. When a gate electrode is supplied with a negative potential, due to repulsive force between a negative charge and a negative charge, carriers (electrons) are away from the TFT section gate electrode 66, as shown in Figure 11(a). Accordingly, the electrons mostly exist in the vicinity of the source and drain electrodes, and few electrons exist in the a-Si layer 68 of the channel section. Thus, the TFT is OFF in this state. Even if the electrons goes from the gate toward the drain, they have to pass the TFT section gate electrode 66. In this case, since the TFT section gate electrode 66 is supplied with a negative potential, the electrons cannot pass through the gate electrode due to

repulsive force between a negative charge and a negative charge. Accordingly, a leak current is small in this arrangement.

[0086]

Meanwhile, in the arrangement shown in Figure 12(a), in which the a-Si layer 68 extends beyond the front end portion of the TFT section gate electrode 66, the electrons can move along the periphery of the a-Si layer 68 without passing through the TFT section gate electrode 66, even when the gate electrode has negative potential. This allows the leak current to easily flow. Further, in the presence of irradiation of backlight, carriers are generated due to excitation by the backlight. For the same reason above, these generated carriers can also flow along the periphery of the a-Si layer 68. Therefore, upon backlight irradiation, the increase amount of the leak current greatly varies between the arrangement of Figures 11(a) with the TFT section gate electrode penetrating through the semiconductor pattern, and in the arrangement of Figures 12(a) with the TFT section gate electrode not penetrating through the semiconductor pattern.

[0087]

As can been seen with the explanation above, it is necessary in the TFT section that the front end of the TFT section gate electrode 66 extends (juts out) beyond the periphery of the a-Si layer 68.

[0088]

Next, the following will explain the case where a positive potential is applied to the gate electrode 13. When a gate electrode 13 is supplied with a positive potential, the electrons in the n+ layer 69 are attracted to the potential of the TFT section gate electrode 66, and therefore carriers exist in the channel section. Therefore, a current can easily flow between the source and drain electrodes, and the TFT is turned on. As one example of this case, a voltage of 10V was applied to the gate electrode. As a result, a current of approximately 1μA flows between the source and drain electrodes. Here, the voltage applied between the source and drain electrodes was 10V. Since the electrons have a behavior to flow in the shortest route between the source and drain electrodes when the TFT is ON, the TFT section gate electrode 66 is not required to penetrate through the semiconductor pattern.

[0089]

However, there arises a problem when the a-Si layer 68 is not balanced with respect to the TFT section gate electrode 66, as shown in Figure 13. Particularly, in the state shown in Figure 13, the drain electrode 18 overlaps with the a-Si layer 68 only in a portion in the width direction. In this case, the flow of electrons are not sufficiently obtained in the source electrode 17, and therefore, the ON current increases or decreases in proportion to the width of the portion of the drain electrode 18 which overlaps with the a-Si layer 68. When having a plurality of such TFTs, the liquid crystal panel has variation of charging condition of each pixel, thus causing unevenness of the image. For this reason, the source electrode 17 and the drain electrode 18 are both required to overlap with the a-Si layer 68, by their whole widths.

[0090]

In this view, in the step for providing the resist layer 67 to be used for processing the a-Si layer 68, by dropping the resist material from the inkjet head 33 of a pattern forming equipment, shooting error (dropping error in the

dropping to a target dropping position), i.e., dropping accuracy needs to be taken into account so as to realize such an arrangement that the a-Si layer 68 entirely overlaps with the source electrode 17 and the drain electrode 18 in the channel section 72 and the front end portion of the TFT section gate electrode 66 is extending out of the a-Si layer 68.

[0091]

Further, in order to create such an arrangement, the shooting error (dropping accuracy) upon dropping of the resist material from the inkjet head 33 of a pattern forming equipment, or more specifically, the dropping accuracy (±10μm, for example) of a pattern forming equipment with respect to the diameter (30μm, for example) of the resist layer 67, needs to be taken into account so as to provide a sufficient length to the TFT section gate electrode 66 so that the front end portion extends out of the a-Si layer 68.

[0092]

Note that, in the example above, the light blocking film (light blocking layer) 62 is formed on a lower portion of the TFT section 22 (in a lower layer than the

semiconductor layer 16); however, the light blocking film 62 may be formed on an upper portion of the TFT section 22 (in an upper layer than the semiconductor layer 16). Here, the following will explain the case where the light blocking film 62 is formed on an upper portion of the TFT section 22, with reference to Figures 14(a) through 14(d). Figure 14(a) is a vertical cross-sectional view showing the TFT array substrate 11 after the partial oxidation treatment of the channel section 72 is completed, and Figure 14(b) is a vertical cross-sectional view of the TFT array substrate 11 showing the step for forming a light blocking film 62 on an upper portion, and Figure 14(c) is a cross-sectional view, taken along the lines M-M of Figure 14(d), and Figure 14(d) is a plan view of the TFT array substrate 11 having the upper light blocking film 62 and showing a state where forming of a pixel electrode 21 is completed.

[0093]

As explained in the gate pre-processing step 41, the light blocking film 62 is optional. For a particular example, a light blocking film 62 formed on an upper layer than the channel section 72 can prevent deterioration of

the TFT characteristic, which is caused by unwanted light from the channel section 72. In the following example, the light blocking film is formed both on a lower portion and an upper portion of the TFT section 22. As circumstances demand, the TFT section 22 may include one or both of the upper and lower light blocking films 62.

[0094]

After the partial oxidation treatment of the channel section 72 is completed as shown in Figure 14(a), an upper light blocking film 62 is formed by dropping a droplet of a light blocking film material with a pattern forming equipment, as shown in Figure 14(b). Thereafter, a photosensitive acrylic resin layer 20 is formed, and further, the pixel electrode 21 is formed, as shown in Figure 14(c).

[0095]

The material of the upper light blocking film 62 may be a resin mixed with TiN, as with the lower light blocking film 62 formed under the gate electrode 13 (TFT section gate electrode 66). Note that, since the light blocking film 62 is formed on an electrode in this example, it is preferable that the light blocking film 62 is made of an

insulation material, and does not include components causing deterioration of performance of the semiconductor layer 16 by diffusing in the semiconductor layer 16.

[0096]

Further, the light blocking film 62 may be formed between a protection layer (not shown) on the TFT and the photosensitive acrylic resin layer 20. This structure provides such an advantage that, since an inter-layer insulation layer is provided between the source and drain electrodes 17 and 18, and the light blocking film 62, the material of the light blocking film 62 is not required to be an insulator, or not required to be decided in consideration of the diffusion of the components in the semiconductor layer, thus widening the choice of materials. Further, in this case, since the photosensitive acrylic resin layer 20, which is used for forming the pixel electrode 21 (ITO electrode), is formed after the light blocking film 62, the level difference which occurs upon forming of the light blocking film 62 can be flattened by providing the photosensitive acrylic resin layer 20 thereon. Therefore, the thickness of the liquid crystal layer becomes even, and prevents occurrence of unevenness of

the display. Further, the light blocking film 62 may be formed before applying ITO to form the pixel electrode 21, i.e., it may be formed between the photosensitive acrylic resin layer 20 and the pixel electrode 21.

[0097]

As described, compared to a conventional manufacturing method without an inkjet type pattern forming equipment, the manufacturing method of a TFT array substrate 11 according to the present invention can reduce the number of masks from 5 to 3, thus reducing photolithography processes and number of vacuum deposition devices. On this account, equipment outlay can also be greatly reduced.

[0098]

[Second Embodiment]

Another Embodiment of the present invention is described below with reference to Figures 15 through 21.

A liquid crystal display device according to the present Embodiment includes a pixel shown in Figure 15(a). Note that, Figure 15(a) is a plan view showing a schematic configuration of a pixel of a TFT array substrate. Further, Figure 15(b) is a cross-sectional view, taken

along the line I-I of Figure 15(a).

[0099]

In the TFT array substrate 11 shown in Figures 1(a) and 1(b), the passivation film 19 is formed after the source and drain electrodes 17 and 18, and thereafter, a guide for the pixel electrode is formed by the photosensitive acrylic resin layer 20.

[0100]

In manufacturing of a TFT array substrate 81 to be used for a liquid crystal display device according to the present Embodiment, the source electrode 17 and a drain/pixel electrode 82 are formed on the same layer in either of a guide forming process or hydrophilic/hydrophobic process using a photocatalyst, which are carried out as one manufacturing step. Note that, in the TFT array substrate 81, the drain electrode and the pixel electrode are made of one continuous electrode, and therefore referred to as a drain/pixel electrode 82. Further, the passivation film 83 is formed substantially only on the TFT section 22.

[0101]

Due to such differences in structure and

manufacturing method, the TFT array substrate 11, on one hand, requires a mask in the manufacturing to form the photosensitive acrylic resin layer 20; and the TFT array substrate 81, on the other hand, does not require in the same step, thus requiring a less number of masks. However, in the manufacturing of the TFT array substrate 81, a guide for the pixel electrode (drain/pixel electrode 82) or the hydrophilic/hydrophobic area is formed in the same step for forming a guide for the source electrode 17. Thus, the TFT array substrate 81 has a smaller aperture ratio than that of the TFT array substrate 11.

[0102]

Further, in the TFT array substrate 11, the pixel electrode 21 and a storage capacitor electrode 14 are formed as separate layers. Therefore, the drain electrode 18 extends to the storage capacitor section 23, and the contact hole 24 is formed above the storage capacitor section 23 so as to conduct the drain electrode 18 to the pixel electrode 21. On the other hand, in the TFT array substrate 81, the drain/pixel electrode 82 is provided also as an electrode extending to the storage capacitor section 23.

[0103]

In both the TFT array substrates 11 and 81, in order to prevent the materials of the source electrode and the pixel electrode from splashing to the channel section 72, the source and drain electrodes are formed by dropping the electrode material from the inkjet head 33 to a portion away from the channel section 72. Also, the area for the source and drain electrodes is formed in a taper shape becoming wider toward the channel section 72 so that the electrode material flows toward the channel section 72. An example of this shape is plainly shown in the vicinity of the channel in the drain electrode 18 and the source electrode in Figure 1(a).

[0104]

Further, the a-Si layer 68 may be formed by processing the a-Si forming layer 64 by using a mask, i.e., by using the resist layer 67 formed by a single (one shot) droplet; however, for a structure including a long TFT extending in parallel to the source electrode 17, the resist layer 67 may be formed by two or more droplets (two or more shots) of the material.

[0105]

Next, the following will explain a manufacturing method of the TFT array substrate 81 including a TFT, used for a liquid crystal display device according to the present embodiment.

[0106]

In the present Embodiment, the TFT array substrate 81 is manufactured through, as shown in Figure 16, a gate pre-processing step 41, a gate line applying/forming step 42, a gate insulation layer/semiconductor layer depositing step 43, a semiconductor layer forming step 44, a source and drain/pixel electrodes pre-processing step 91, a source line applying/forming step 92, a drain/pixel electrode applying/forming step 93, a channel section processing step 94, a passivation film forming step 95. The gate pre-processing step 41 through the semiconductor layer forming step 44 are the same as those in manufacturing of the TFT array substrate 11, and therefore explanations thereof will be omitted here.

[0107]

(Source and drain/pixel electrodes pre-processing step 91)

Figure 17 shows the source and drain/pixel electrodes pre-processing step 91. Figure 17 is a plan view showing the glass substrate 12 after the semiconductor layer forming step, i.e., the glass substrate 12 provided with a wiring guide 84 for forming the source electrode 17 and a wiring guide 85 for forming the drain/pixel electrodes 82.

[0108]

In this step, the wiring guide 84 is formed on an area for forming the source electrode 17 (source forming area 86), and the wiring guide 85 is formed in an area for forming the drain/pixel electrodes 82 (drain/pixel electrodes forming area 87). In this Embodiment, the wiring guides 84 and 85 were formed by a photoresist material. More specifically, the glass substrate 12 after the semiconductor layer forming step 44 was coated with a photoresist, and was subjected to pre-baking, and then developed by exposure using a photo mask, and further subjected to post-baking. Each of the wiring guides 84 and 85 thus created had a width = 10μm, and the width of the groove (the width of the wiring forming area) created with the wiring guide 84 was approximately 15μm. Note

that, the interval between the source and drain electrodes, i.e., the channel section 72 was set to 4μm.

[0109]

Note that, here, the glass substrate 12 may be arranged such that the SiNx surface (the upper surface of the gate insulation layer 15) is processed to be provided with hydrophilicity by using an oxygen plasma, and the wiring guides 84 and 85 are processed to be provided with water-repellence by supplying CF_4 plasma, so that the wiring material from a pattern forming equipment can be smoothly applied to the base surface.

[0110]

Further, instead of forming the wiring guides 84 and 85, the glass substrate 12 may be subjected to the hydrophilic/hydrophobic processing using a photocatalyst according to the pattern of wiring electrode, as with the foregoing gate electrode forming step. Note that, in this case, a particular care is required to prevent the material of the source electrode from being splashing to the pixel electrode.

[0111]

(Source line applying/forming step 92)

Figures 18(a) and 18(b) show the source line applying/forming step 92. Figure 18(a) is a plan view showing the source electrode 17 which has been formed along the wiring guide 84. Figure 18(b) is a cross-sectional view, taken along the line J-J of Figure 18(a).

[0112]

As shown in Figures 18(a) and 18(b), in this source line applying/forming step 92, the source electrode 17 was formed by coating the source forming area 86, which is formed by the wiring guide 84, with a wiring material by using a pattern forming equipment. Here, the discharging amount of the wiring material from the inkjet head 33 was set to 2pl. Further, Ag particles are used as the wiring material, and the thickness of the electrode was adjusted to 0.3μm. Further, baking temperature was 200°C, and after the baking, the wiring guide 84 was removed by an organic solvent.

[0113]

Note that, in this step, the same wiring material may be used as the one used for the gate electrode 13; however, the baking temperature is required to be at or lower than

300°C, since the a-Si is formed at around 300°C.

[0114]

(Drain/pixel electrode applying/forming step 93)

Figure 19(a) and 19(b) show the drain/pixel electrode applying/forming step 93. Figure 19(a) is a plan view showing the drain/pixel electrode 82 which has been formed along the wiring guide 85. Figure 19(b) is a cross-sectional view, taken along the line K-K of Figure 19(a).

[0115]

In this drain/pixel electrode applying/forming step 93, the drain/pixel electrode 82 was formed by applying an ITO particle material to the wiring guide 85 by using a pattern forming equipment, and then was baked with a baking temperature of 200°C.

[0116]

In this manner, only a single mask is required for the source/drain electrodes forming step and the ITO processing step, unlike the conventional method which uses respective masks for these steps. Further, the use of an inkjet type pattern forming equipment allows separate application of the electrode material and the

pixel electrode material with respect to each pattern by using separate inkjet heads 33. Accordingly, the present method requires a simpler device system and improves efficiency of material use, thus realizing cost reduction.

[0117]

(Channel section processing step 94)

This step is carried out for processing the channel section 72 of the TFT. Figures 20(a) and 20(b) are cross-sectional views corresponding to a portion taken along the line K-K of Figure 19(a). Firstly, as shown in Figure 20(a), the wiring guides 84 and 85 of the channel section 72 were removed by an organic solvent or by ashing. Next, as shown in Figure 20(b), the n+ layer 69 was subjected to oxidation treatment by ashing or by using a laser so as to be a nonconductor.

[0118]

(Passivation film forming step 95)

Figure 21 shows the passivation film forming step 95. Figure 19(a) is a cross-sectional view corresponding to a portion taken along the line K-K of Figure 19(a). In this step, a passivation film 83 was formed by a pattern forming equipment on a glass substrate 12 which had

been provided with the source electrode 17 and the drain/pixel electrode 82. To create the passivation film 83, a transparent inorganic material such as an ethoxy silane material is applied on the TFT section 22, and then was baked with a temperature of approximately 150°C. The material of the passivation film 83 may also be a resist material or a photosensitive resin. Further, the light blocking film 62 may be used as the material which blocks external light and also operates as black matrix on a color filter. Namely, both a transparent material and an opaque material may be used as the material of the passivation film 83. Here, a TFT array substrate 81 is completed.

[0119]

In comparison with the conventional manufacturing without an inkjet method, the number of masks may be reduced from 5 to 2 in the manufacturing steps of the present embodiment, and the source electrode 17 and the drain/pixel electrode 82 can be formed by one guide forming step. Therefore, the number of masks can further be reduced less than that of the manufacturing of the TFT array substrate 11. Further, as with the

manufacturing of the TFT array substrate 11, number of vacuum deposition equipments can be reduced.

[0120]

Note that, the foregoing example uses a-Si for the semiconductor layer; however, an organic semiconductor or a particle type semiconductor material may also be used. In this case, a step for directly applying a semiconductor material from a pattern forming equipment is carried out instead of the processing step of a-Si of the TFT array substrate. Accordingly, application of a resist or resin material, dry etching, and removal process of the resist or resin material can be omitted, thereby further simplifying the manufacturing.

[0121]

Figures 22(a) through 22(c) show a manufacturing method of the semiconductor layer 16 according to the foregoing manner.

In this manner, after forming the gate insulation layer 15, a semiconductor material is directly dropped from a pattern forming equipment onto the gate insulation layer 15 in the TFT section 22, and the material is then baked to create the semiconductor layer 16, as shown in

Figures 22(b) and 22(c). In this example, an organic semiconductor material such as polyvinyl carbazole (PVK) or polyphenylene vinylene (PPV) may be used as the semiconductor material.

[0122]

In contrast to an a-Si formed by a CVD, etching process is not necessary to the foregoing materials since they can be formed to be the semiconductor layer 16 with a droplet (1 shot) from a pattern forming equipment. Thus, hydrophilic/hydrophobic processing is not necessary in the area for forming the semiconductor layer 16, in this case.

[0123]

The TFT array substrates 11 and 18 described in Embodiments 1 and 2 was arranged so that the gate electrode 13 includes the TFT section gate electrode 66, which is branched out from the main line of the gate electrode 13; and the TFT was formed on this TFT section gate electrode 66. In this example, the gate electrode 13 does not include a branch electrode (TFT section gate electrode 66).

[0124]

As shown in Figure 23, the semiconductor layer 16 is formed on the gate electrode 13 (gate line), and a branch electrode 17a from the source electrode 17 extends to the channel section 72 (TFT section 72). Meanwhile, the drain electrode 18 linearly extends from the storage capacitor section 23 constituting the storage capacitor, and reaches to the channel section 72. Note that, this example has been explained as an arrangement compatible with the First Embodiment shown in Figure 1; however, this example may also be adopted for the Second Embodiment shown in Figure 15.

[0125]

In the TFT array substrate 11 of this example, since the gate electrode 13 does not include a branch electrode, the foregoing arrangement with a branch electrode (TFT section gate electrode 66) penetrating through the semiconductor pattern is not necessary.

[0126]

This arrangement of the TFT array substrate 11 is effective for a configuration where the gate electrode 13 has relatively narrow width, for example in a range between 10μm and 20μm. In a display panel of at or less

than a range of 10-15 inches in diagonal screen measurement, the gate electrode 13 is formed with a relatively narrow width and short length. On the other hand, in a display panel of at or larger than 20 inches, the width of the gate electrode 13 becomes wider for reducing the resistance. If the present example is adopted in this case, the width of the gate electrode in the TFT forming area needs to be narrow. Namely, the present arrangement is effective in a case where the length of the TFT is substantially same as the width of the gate electrode.

[0127]

Note that, since there also are influences of the resistance of materials and other design parameters, the foregoing relation between the size of the screen and the width of the gate electrode is not always true.

[0128]

Further, in the foregoing explanation, the shape of the droplet refers to a state of a droplet when dropped from a pattern forming equipment. The contour of this shape has a curvature. Therefore, if only one droplet is dropped, or plural droplets are dropped onto the same

position, the shape of the droplet becomes a circular or a substantially circular shape, as shown in Figure 24.

[0129]

Further, the shape of the droplet is not always a circular or a substantially circular shape but can be a deformed circular shape (a collapsed or distorted circle). For example, the shape may be a substantially circular shape deformed from a circle, as shown in Figure 25(a), a shape having a concave portion, as shown in Figure 25(b), a shape partly including a convex portion, as shown in Figure 25(c). It is assumed that such a shape with a contour having a curvature is created due to delicate difference of surface condition of the substrate on which the droplet is dropped, or due to air resistance when the droplet splashes. The foregoing shapes all satisfy the regulation of the present invention for the shape of droplet, because they each are regarded immediate shapes created by dropping.

[0130]

Further, the shape of droplet is not necessarily created by a single droplet but by plural droplets. Figure 26(a) shows a case where a deformed oval shape is formed

by two droplets. The respective droplets merge as a result of dropping, or merge into a contour after dropping, and result in a shape with a contour having a curvature. Figure 26(b) shows an example formed by three droplets.

[0131]

It should be noted that the present example do not intend the state shown in Figure 27(a) where a plural of infinitesimal droplets are applied, which results in the shape shown in Figure 27(b).

[0132]

The present invention is not limited to the aforementioned embodiments and is susceptible of various changes within the scope of the accompanying claims. Also, an embodiment obtained by suitable combinations of technical means disclosed in the different embodiments are also include within the technical scope of the present invention.

[0133]

[EFFECTS OF THE INVENTION]

As described, the TFT array substrate according to the present invention includes a semiconductor layer having a shape formed by dropping a droplet.

[0134]

On this account, the manufacturing of the TFT array substrate can be performed without a mask for forming a semiconductor layer. As a result, the number of masks is reduced, thus reducing manufacturing processes. Further, the manufacturing requires less photolithography processes using a mask, thus reducing equipment outlay for the photolithography and amount of waste material. This allows reduction of time and costs of manufacturing.

[0135]

The TFT array substrate may have such an arrangement that the gate electrode in the thin film transistor section is a branch electrode which is branched out of a main line of the gate electrode, and the branch electrode has an open end protruded from an area for the semiconductor layer.

[0136]

With the foregoing arrangement, since the open-end of the branch electrode of the thin film transistor section is protruded from the area for the semiconductor layer, a leak current between the source and drain electrodes can be appropriately suppressed by the electrical field from

the branch electrode.

[0137]

The foregoing TFT array substrate may have such an arrangement that the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the source and drain electrodes each have an end that is positioned closer to the channel section, and confined over an entire width within the area for the semiconductor layer.

[0138]

With the foregoing arrangement, the source electrode of each pixel can be supplied with a sufficient ON current, thus preventing nonuniformity of charging condition of the pixel, which causes unevenness of the image.

[0139]

The TFT array substrate according to the present invention may have such an arrangement that the thin film transistor section further includes a light-blocking film on either of an upper layer or an lower layer of the semiconductor layer, the light-blocking film having a shape formed by dropping a droplet, and being formed on

a portion corresponding to the position of the semiconductor layer.

[0140]

With the foregoing arrangement, when the light-blocking film is required, it can be created easily by dropping a droplet(s) of a light-blocking film material by using an inkjet method or the like. Accordingly, as with the forming of the semiconductor layer, the light-blocking film can be formed without a mask. On this account, it is not necessary to use extra number of masks or larger amount of material in the manufacturing of the TFT array substrate, thus reducing manufacturing steps and costs.

[0141]

The liquid crystal display device of the present invention includes the foregoing TFT array substrate. Therefore, the manufacturing of the liquid crystal display requires less number of masks, thus reducing time and costs of manufacturing.

[0142]

A manufacturing method of the TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a

gate insulation layer on the gate electrode; (c) depositing a semiconductor film on the gate insulation layer; (d) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and (e) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor layer of a thin film transistor section.

[0143]

In this manner, a resist layer is formed on a deposited semiconductor film by dropping a droplet of a resist material, and the semiconductor layer is formed by using this resist layer having the shape of the droplet (normally a circular shape) as a mask.

[0144]

Accordingly, the forming of the semiconductor layer does not require a mask, and therefore, the total required number of masks is reduced, thus reducing manufacturing processes. Further, since the manufacturing requires less photolithography processes using a mask, it is possible to reduce equipment outlay for the photolithography and amount of waste material.

This allows reduction of time and costs of manufacturing.

[0145]

A manufacturing method of the TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; and (c) forming a semiconductor layer having a shape of a droplet as a semiconductor layer of a thin film transistor section, by dropping a droplet of a semiconductor material on the gate insulation layer on the branch electrode.

[0146]

In this manner, the semiconductor layer is formed in a shape of a droplet (normally a circular shape) by only dropping a droplet of a semiconductor material on the gate insulation layer of the branch electrode.

[0147]

Accordingly, the forming of the semiconductor layer does not require a mask, and therefore, the total required number of masks is reduced, thus reducing manufacturing processes. Further, since the manufacturing requires less photolithography processes using a mask, it is possible to reduce equipment outlay

for the photolithography and amount of waste material. This allows reduction of time and costs of manufacturing.

[0148]

The foregoing manufacturing method of the TFT array substrate according to the present invention may be arranged so that: in the step (a), the gate electrode is formed so that the gate electrode includes a main line and a branch electrode branched out of the main line, the branch electrode having an open end protruded from an area for the semiconductor layer.

[0149]

With the foregoing arrangement, since the branch electrode of the gate electrode of the thin film transistor section has an open-end protruded from the area for the semiconductor layer, a leak current between the source and drain electrodes can be appropriately suppressed by the electrical field from the branch electrode.

[0150]

The foregoing manufacturing method of the TFT array substrate may be arranged so that: the branch electrode is specified by length according to dropping accuracy of the droplet so that the open end is protruded from the area

for the semiconductor layer.

[0151]

In this manner, the droplet of a resist material or a semiconductor material is dropped in a position for allowing the open-end of the branch electrode to be protruded from the area for the completed semiconductor. Thus, the leak current between the source and drain electrodes can be appropriately suppressed.

[0152]

A manufacturing method of a TFT array substrate according to the present invention includes the steps of: (a) forming a gate electrode on a substrate; (b) forming a gate insulation layer on the gate electrode; (c) forming a semiconductor layer of a thin film transistor section on the gate insulation layer; (d) forming a first area to which a source electrode is formed, and a second area to which at least a pixel electrode is formed, by dropping a droplet of an electrode material on the substrate after subjected to the step (c); and (e) forming a source electrode, a drain electrode, and a pixel electrode in the first and the second areas by dropping droplets of an electrode material on the substrate after subjected to the step (d).

[0153]

In this manner, the first area to which a source electrode is formed by dropping a droplet of an electrode material, and the second area to which at least a pixel electrode is formed by dropping a droplet of an electrode material are formed in one process for pre-processing of the electrode forming step. Therefore, the manufacturing processes and costs can be reduced compared to the case of separately forming the first and the second areas in different steps.

[0154]

A manufacturing method of a liquid crystal display device according to the present invention includes one of the foregoing manufacturing methods of a TFT array substrate. Therefore, it is possible to reduce at least manufacturing processes for producing a liquid crystal display device, thus reducing costs.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIGURE 1]

Figure 1(a) is a plan view showing a schematic configuration of a pixel of a TFT array substrate in a liquid crystal display device according to one Embodiment

of the present invention, and Figure 1(b) is a cross-sectional view, taken along the line A-A of Figure 1(a).

[FIGURE 2]

Figure 2 is a perspective view schematically showing a pattern forming equipment using an inkjet method, and is used for manufacturing of a liquid crystal display device according to one Embodiment of the present invention.

[FIGURE 3]

Figure 3 is a flow chart showing manufacturing steps of the TFT array substrate shown in Figure 1.

[FIGURE 4]

Figure 4(a) is a plan view of a TFT array substrate for explaining the gate pre-processing step shown in Figure 3, Figure 4(b) is a plan view of a TFT array substrate for explaining the gate line applying/forming step, and Figure 4(c) is a cross-sectional view, taken along the line B-B of Figure 4(b).

[FIGURE 5]

Figures 5(a) through 5(c) are cross-sectional views corresponding to a portion taken along the line B-B of

Figure 4(b), and Figure 5(a) shows the gate insulation layer/semiconductor layer depositing step, Figure 5(b) shows how a thermosetting resin is formed on the semiconductor layer in the semiconductor layer forming step shown in Figure 3, Figure 5(c) shows an etching process of the a-Si forming layer and the n+ forming layer in the same step, and Figure 5 (d) is a cross-sectional view, taken along the line C-C of Figure 5(e), showing a resist removal process in the same step, and Figure 5(e) is a plan view of a TFT array substrate after the semiconductor layer forming step.

[FIGURE 6]

Figure 6(a) is a plan view of a TFT array substrate for explaining the source/drain lines pre-processing step shown in Figure 3, Figure 6(b) is a plan view of a TFT array substrate for explaining the source/drain lines applying/forming step, Figure 6(c) is a cross-sectional view, taken along the line D-D of Figure 6(b).

[FIGURE 7]

Figure 7 is a plan view showing a TFT section in the TFT array substrate shown in Figure 1(a).

[FIGURE 8]

Figures 8(a) and 8(b) are cross-sectional views corresponding to a portion taken along the line D-D of Figure 6(b), and Figure 8(a) shows removal process of wiring guide in the channel section processing step shown in Figure 3, and Figure 8(b) shows oxidation treatment of the n+ layer in the same step.

[FIGURE 9]

Figure 9(a) is a plan view of a TFT array substrate for explaining the passivation film forming step and the passivation film processing step, which are shown in Figure 3, and Figure 9(b) is a cross-sectional view, taken along the line E-E of Figure 9(a).

[FIGURE 10]

Figure 10(a) is a plan view of a TFT array substrate for explaining the pixel electrode forming step shown in Figure 3, and Figure 10(b) is a cross-sectional view, taken along the line F-F of Figure 10(a).

[FIGURE 11]

Figures 11(a) and 11(b) are explanatory views showing mechanism of occurrence of a leak current in the TFT section shown in Figure 1(a), and Figure 11(a) is a plan view showing the TFT section with the gate electrode

penetrating through the semiconductor pattern, and Figure 11(b) is a cross-sectional view, taken along the line G-G of Figure 11(a).

[FIGURE 12]

Figure 12(a) is a plan view of the TFT section in which the gate electrode does not penetrate through the semiconductor pattern, in contrast to the configuration of Figure 11(a), for showing the mechanism of occurrence of a leak current, and Figure 12(b) is a cross-sectional view, taken along the line H-H of Figure 12(a).

[FIGURE 13]

Figure 13 is a plan view showing the TFT section shown in Figure 1(a) when the a-Si layer is not balanced with respect to the gate electrode.

[FIGURE 14]

Figure 14(a) is a vertical cross-sectional view for explaining a manufacturing method of the TFT array substrate having an upper light blocking film in addition to a lower light blocking film, and shows a state of the TFT array substrate when a partial oxidation treatment of the channel section is completed, Figure 14(b) is a vertical cross-sectional view of the TFT array substrate showing

the step for forming an upper light blocking film, Figure 14(c) is a cross-sectional view, taken along the lines M-M of Figure 14(d), and Figure 14(d) is a plan view of the TFT array substrate showing a state where forming of a pixel electrode is completed.

[FIGURE 15]

Figure 15(a) is a plan view showing a schematic configuration of a pixel of a TFT array substrate in a liquid crystal display device according to another Embodiment of the present invention, and Figure 15(b) is a cross-sectional view, taken along the line I-I of Figure 15(a),

[FIGURE 16]

Figure 16 is a flow chart showing manufacturing steps of the TFT array substrate shown in Figures 15(a) and 15(b).

[FIGURE 17]

Figure 17 is a plan view of a TFT array substrate for explaining the source and drain/pixel electrodes pre-processing step shown in Figure 16.

[FIGURE 18]

Figure 18(a) is a plan view of a TFT array substrate

for explaining the source line applying/forming step shown in Figure 16, and Figure 18(b) is a cross-sectional view, taken along the line J-J of Figure 18(a).

[FIGURE 19]

Figure 19(a) is a plan view for explaining the drain/pixel electrodes applying/forming step shown in Figure 16, Figure 19(b) is a cross-sectional view, taken along the line K-K of Figure 19(a).

[FIGURE 20]

Figures 20(a) and 20(b) are cross-sectional views corresponding to a portion taken along the line K-K of Figure 19(a), and Figure 20(a) shows removal process of a wiring guide in the channel section processing step shown in Figure 16, and Figure 20(b) shows an oxidation treatment of the n+ layer in the same step.

[FIGURE 21]

Figure 21 is a cross-sectional view corresponding to a portion taken along the line K-K of Figure 19(a) for explaining the passivation film forming step shown in Figure 16.

[FIGURE 22]

Figure 22(a) is a cross-sectional view showing a TFT

array substrate according to still another Embodiment of the present invention, and shows a state of the TFT array substrate before provided with a semiconductor layer, Figure 22(b) is a cross-sectional view, taken along the line L-L of Figure 22(c), showing the TFT array substrate provided with a semiconductor layer, and Figure 22(c) is a plan view showing the TFT array substrate provided with a semiconductor layer.

[FIGURE 23]

Figure 23 is a plan view showing a schematic configuration of a pixel of a TFT array substrate in a liquid crystal display device according to yet another Embodiment of the present invention.

[FIGURE 24]

Figure 24 is an explanatory view showing a droplet having substantially a round shape, as an example of the shape of droplet dropped from the pattern forming equipment shown in Figure 2.

[FIGURE 25]

Figure 25 (a) is an explanatory view showing a droplet having a substantially circular shape by being deformed from a circle, as another example of the shape of

the droplet shown in Figure 24, Figure 25(b) is an explanatory view showing a shape having a concave portion, and Figure 25(c) is an explanatory view showing a shape partly including a convex portion.

[FIGURE 26]

Figure 26(a) shows a case where an irregular oval shape is formed by two droplets, and Figure 26(b) is an explanatory view showing a shape formed by three droplets.

[FIGURE 27]

Figure 27 (a) is an explanatory view showing a state, which is not desired in the present invention, where plural infinitesimal droplets are dropped, and Figure 27(b) is an explanatory view showing a shape formed by the state of Figure 27(a).

[FIGURE 28]

Figure 28 is a flow chart showing manufacturing steps of a TFT array substrate for a conventional liquid crystal display device.

[REFERENCE NUMERALS]

11 TFT array substrate

12 glass substrate

13 gate electrode

14 storage capacitor electrode

15 gate insulation layer

16 semiconductor layer

17 source electrode

18 drain electrode

19 passivation film

20 photosensitive acrylic resin layer

21 pixel electrode

22 TFT section

23 storage capacitor section

24 contact hole

33 inkjet head

61 gate line forming area

62 light blocking film

64 a-Si forming layer

65 n+ forming layer

66 TFT section gate electrode (branch electrode)

67 resist

68 a-Si layer

69 n+ layer

71,84,85 wiring guide

72 channel section

73	source/drain forming area
81	TFT array substrate
82	drain/pixel electrode
83	passivation film
86	source forming area
87	drain/pixel electrodes forming area

[TITLE OF THE DOCUMENT] ABSTRACT

[ABSTRACT]

[OBJECT]

To enable the reduction of manufacturing steps and costs by using an inkjet method, for example.

[MEANS TO ACHIEVE THE OBJECT]

A TFT array substrate 11 includes a thin film transistor section 22 in which a gate electrode 13 is formed on a glass substrate 12, and a semiconductor layer 16 is formed via a gate insulation layer 15 on the TFT section gate electrode 66, which is branched out from the main line of the gate electrode 13. The semiconductor layer 16 of this TFT array substrate 11 has a shape formed by dropping a droplet. Accordingly, it is possible to directly form a semiconductor layer, or a resist layer for forming the semiconductor layer, by dropping a droplet(s).

[SELECTED DRAWINGS] Fig. 1